Customer No.: 31561
Docket No.: 13714-US-PA
Application No.: 10/711,673

REMARKS

Present Status of Application

The Office Action dated May 02, 2005, rejected claims 1-20 under 35 USC§102(b) as being anticipated by Herbert (US Patent No. 6,528,850).

Claims 1 and 11 have been amended for providing more descriptions. No new matter has been added to the application by the amendments made to the specification, claims and drawings. This Amendment is promptly filed to place the above-captioned case in condition for allowance. After entering the amendments and considering the following discussions, a notice of allowance is respectfully solicited.

Discussion for 35 USC§102 rejections

Claims 1-20 were rejected under 35 USC§102(b) as being anticipated by Herbert (US Patent No. 6,528,850).

The Office Action considered that Herbert substantially disclosed this invention.

Claims 1 and 11 have been amended to provide more descriptions for clarification purposes, according to the present invention. Supporting grounds for this amendment can be found at least in figures 9-10 and the related descriptions in the specification.

Applicants submit that amended independent claims 1 and 11 patently define over the prior references for at least the reason that the cited art fails to disclose each and every

feature as claimed in the present invention.

The independent claims 1 and 11 recites respectively:

Claim 1.A high voltage device for an electrostatic discharge protection circuit, comprising:

a first type substrate;

a first type epitaxial silicon layer disposed in the first type substrate;

a first type well disposed in the first type epitaxial silicon layer;

a second type well disposed in the first type epitaxial silicon layer, wherein the second type well comprises a second type lightly doped region and a second type heavily doped region, the second type lightly doped region is located next to the first type well and the second heavily doped region is located underneath a portion of the first type well and the second type lightly doped region, wherein the first type well adjoins with the second heavily doped region;

a gate structure disposed on a portion of the first type well and the second type lightly doped region;

a second type first doped region and a second type second doped region disposed in the second type lightly doped region and the first type well on each side of the gate structure respectively;

a first isolation structure disposed in the second type lightly doped region and between the gate structure and the second type first doped region; and

a first type doped region disposed in the first type well and adjacent to the second type second doped region.

Claim 11. A high voltage device, comprising:

a first type substrate;

a first type epitaxial silicon layer disposed in the first type substrate;

a first type well disposed in the first type epitaxial silicon layer;

a second type well disposed in the first type epitaxial silicon layer, wherein the second type well comprises a second type lightly doped region and a second type heavily doped region, the second type lightly doped region is located next to the first type well and the second heavily doped region is located underneath a portion of the first type well and the second type lightly doped region, wherein the first type well adjoins with the second heavily doped region;

a gate structure disposed on a portion of the first type well and the second type lightly doped region;

a second type first doped region and a second type second doped region disposed in the second type lightly doped region and the first type well on each side of the gate structure respectively;

a first isolation structure disposed in the second type lightly doped region and between the gate structure and the second type first doped region; and

a first type doped region disposed in the first type well and adjacent to the second type second doped region.

Applicant respectfully asserts that claim 1 or 11 is patentably distinct from the prior art structures, especially at least "wherein the first type well adjoins with the second heavily doped region".

Herbert merely discloses a high voltage MOS transistor. As described in Herbert's Fig. 1B, a high voltage DMOS transistor 20 with an **isolated body** is shown. The DMOS transistor 20 includes N+ source region 22, N+ drain region 27, P-type body region 24, gate 21, thick oxide 25, P-type epitaxial layer 26, P-type substrate 29, N-type well 23 and N+ buried layer 28 (col. 1, lines 62-col. 2, line 1). Clearly, P-type body region 24 is isolated from N+ buried layer 28; namely, P-type body region 24 is physically not connected with N+ buried layer 28.

The Office Action considered Herbert's P-type body region 24 and N+ buried layer 28 being respectively comparable to the first type well and the second type heavily doped region of this application. Applicant respectfully disagrees with this consideration.

Even if considering Herbert's N+ buried layer 28 being comparable to the second type heavily doped region of this application, Herbert fails to teach or suggest the first type well that adjoins with the second heavily doped region, as recited in claim 1 or 11. Contrarily, the underfill material 240 is applied to the surface of the substrate 250. Furthermore, Herbert mentioned nothing related to "the PN junction between the second

type heavily doped region and the first type well has a smaller breakdown voltage than the PN junction between the second type lightly doped region and the first type well, and the breakdown voltage of the PN junction between the second type heavily doped region and the first type well is the breakdown voltage of the electrostatic discharge protection circuit".

Accordingly, the structure of the present invention is patentably distinct from the prior art reference Herbert because Herbert fails to disclose all limitations of independent claim 1 or 11. As a result, Herbert did not anticipate the present invention as suggested by the Office Action, to arrive at the present invention as recited in independent claim 1 or 11. For at least the foregoing reasons, all pending claims patently define over the cited reference and should be allowed.

Consequently, reconsideration and withdrawal of these 102 rejections are respectfully requested.

Customer No.: 31561
Docket No.: 13714-US-PA
Application No.: 10/711,673

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : August 1, 2005

Respectfully submitted,

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw